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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,531	11/13/2003	Chin-Lin Liu	MXIC-P920186	2193

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EXAMINER	
KENNEDY, JENNIFER M	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/714,531	LIU ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-13,16-19 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13, 16-19, 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-13, 16-19, and 22 in the reply filed on June 18, 2004 is acknowledged.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 6-7, 9-11, 13, 16-19, and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Lung et al. (U.S. Patent Appl. 2003/0106489).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In re claim 1, Lung et al. discloses the method for fabricating a ferroelectric capacitor in an integrated circuit, the method comprising: fabricating a metal-oxide-semiconductor transistor (see [0029]; CMOS) on a substrate; depositing an insulating layer (120) on the metal-oxide-semiconductor transistor; depositing a conducting layer

on the insulating layer using a low temperature process (130, 140; see [0030]); and depositing a ferroelectric layer (150, see [0031]) on the conducting layer using a low temperature process.

In re claim 2, Lung et al. discloses the method wherein the depositing of an insulating layer comprises depositing a silicon dioxide layer (120, see [0029]).

In re claim 3, Lung et al. discloses the method wherein the depositing of a conducting layer on the insulating layer comprises: depositing a first conducting layer (130) on the insulating layer; and depositing a second conducting layer (140) on the first conducting layer.

In re claim 4, Lung et al. discloses the method wherein the depositing of a first conducting layer comprises depositing a platinum layer (130, see [0030]).

In re claim 6, Lung et al. discloses the method wherein the depositing of a second conducting layer comprises depositing a layer of conducting oxide (140, see [0030]).

In re claim 7, Lung et al. discloses the method wherein the depositing of a layer of conducting oxide comprises depositing a layer of lanthanum nickel oxide ($LaNiO_3$) (140, see [0030]).

In re claim 9, Lung et al. discloses the method wherein the depositing of a layer of lanthanum-nickel oxide comprises depositing lanthanum nickel oxide by sputtering at a temperature of about 350^{o}C (see Table 1).

In re claim 10, Lung et al. discloses the method wherein the depositing of a layer of lanthanum nickel oxide comprises causing the lanthanum nickel oxide to form a perovskite phase (see [0043]) .

In re claim 11, Lung et al. discloses the method wherein the depositing of a ferroelectric layer comprises depositing a lead zirconate titanate layer (150, see [0031]).

In re claim 13, Lung et al. discloses the method wherein the depositing of a lead zirconate titanate layer comprises depositing a lead zirconate titanate layer using a process that operates at a temperature substantially in a range of about 450 ^{o}C to about 550 ^{o}C (see Table 2).

In re claim 16, Lung et al. discloses a manufacturing method for fabricating a ferroelectric capacitor in an integrated circuit, the method comprising: fabricating a metal-oxide-semiconductor transistor on a substrate (CMOS, see [0029]); depositing an insulating layer (120) on the metal-oxide-semiconductor; depositing a conducting layer (130, 140) on the insulating layer using a process to cause at least part of the conducting layer to form a perovskite phase (see [0043]); and depositing a ferroelectric layer on the conducting layer using a process to cause at least part of the ferroelectric layer to form a perovskite phase (150, see [0043]).

In re claim 17, Lung et al. discloses the method wherein the depositing of a conducting layer on the insulating layer comprises: depositing a first conducting layer

(130) on the insulating layer; and depositing a second conducting layer (140) on the first conducting layer.

In re claim 18, Lung et al. discloses the method wherein the depositing of a conducting layer on the insulating layer is performed using a low temperature process (see Table 1). The applicant defines sputtering and MOCVD as low temperature processes. Further the examiner notes the temperatures at which Lung et al. performs the sputtering is at 350 °C, which is the same temperature at which the applicant performs their low temperature process.

In re claim 19, Lung et al. discloses the method wherein the depositing of a ferroelectric layer on the conducting layer is performed using a low temperature process (see Table 2). The applicant defines sputtering and MOCVD as low temperature processes. Further, the examiner notes the temperatures at which Lung et al. performs the sputtering is at 450 °C, which is the same temperature at which the applicant performs their low temperature process.

In re claim 22, Lung et al. discloses the method wherein the depositing of a ferroelectric layer comprises depositing a lead zirconate titanate layer (150, see [0031]).

Claims 1-3, 5-6, 8, and 11-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Inoue et al. (U.S. Patent No. 6,146,906).

In re claim 1, Inoue et al. discloses the method for fabricating a ferroelectric capacitor in an integrated circuit, the method comprising: fabricating a metal-oxide-semiconductor transistor (103, 104) on a substrate; depositing an insulating layer (107) on the metal-oxide-semiconductor transistor; depositing a conducting layer (108, 109) on the insulating layer using a low temperature process (see column 5, lines 19-25); and depositing a ferroelectric layer (110) on the conducting layer using a low temperature process (see column 5, lines 30-40).

The examiner notes the applicants define MOCVD and sputtering as low temperature processes.

In re claim 2, Inoue et al. discloses the method wherein the depositing of an insulating layer comprises depositing a silicon dioxide layer (107, BPSG, a doped silicon oxide).

In re claim 3, Inoue et al. discloses the method wherein the depositing of a conducting layer on the insulating layer comprises: depositing a first conducting layer (108) on the insulating layer; and depositing a second conducting layer (109) on the first conducting layer.

In re claim 5, Inoue et al. discloses the method wherein the depositing of a first conducting layer comprises depositing an iridium layer (see column 5, lines 5-21, specifically Ir/ IrO_2).

In re claim 6, Inoue et al. discloses the method wherein the depositing of a second conducting layer comprises depositing a layer of conducting oxide (see column 5, lines 5-21, specifically Ir/ IrO_2).

In re claim 8, Inoue et al. discloses the method wherein the depositing of a layer of conducting oxide comprises depositing a layer of iridium oxide (IrO_2) (see column 5, lines 5-21, specifically Ir/ IrO_2).

In re claim 11, Inoue et al. discloses the method wherein the depositing of a ferroelectric layer comprises depositing a lead zirconate titanate layer (110, see column 5, lines 30-40).

In re claim 12, Inoue et al. discloses the method wherein the depositing of a lead zirconate titanate layer comprises depositing a lead zirconate titanate layer using metal organic chemical vapor deposition (110, see column 5, lines 30-40).

In re claim 13, Inoue et al. discloses the method wherein the depositing of a lead zirconate titanate layer comprises depositing a lead zirconate titanate layer using a process that operates at a temperature substantially in a range of about 450 ^{o}C to about 550 ^{o}C (110, see column 5, lines 30-40).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Patent Examiner
Art Unit 2812

jmk